Method of Fabricating Thin Film Transistor TFT Array

Field of the Invention

The present invention relates to the method of fabricating thin film transistor TFT array. It uses the theory of oxidation-reduction to manufacture metal wiring for implementing the metal wiring layout of the TFT-LCDs.

Background of the Invention

The quality of the technique is enhancing constantly, therefore, people has more requirements on their life quality. Monochrome display monitor cannot meet for present image industry. Further, the cathode-ray tube CRT has gradually been replaced by the flat panel display FPT as well as the expensive plasma panel display PPD in the color display monitor.

In order to enhance the competition for the products in the liquid crystal display LCD, the latest display panel has been researched constantly. This may include thin-film transistor liquid crystal display TFT-LCD. The conventional TFT-LCD is used in the big-area application, and therefore, the delay phenomenon caused from the resistor capacitor RC influences the result of the image display.

More, the conventional metal wiring process uses expensive physical vapor deposition method PVD, and therefore, the

manufacturing cost in the TFT-LCD is more expensive. Apart from this, the consequent thin film process such as etching and high-temperature tempering of the low resistance metal which is with high diffusion such as Cu, has more troublesome thereto causes component defects. As a result, the present invention can overcome the problem of the conventional technique.

Summary of the Invention

The present invention relates to the method of fabricating thin film transistor TFT array. It uses the theory of oxidation- reduction to manufacture metal wiring for implementing the metal wiring layout of the TFT-LCDs. More, it decreases the times of the high-diffusion wiring exposure in the masking process thereto decreases the component defects from the metal wiring while processing in the multiple masking processes.

The present invention uses A-Si layer as a seed layer. Then, it uses the low-resistance metal with stronger oxidation ability for Si as well as uses the chemical plating method to implement the metal wiring layout of the TFT-LCDs. This, therefore, can replace the lithography etching method being used in the metal wiring layout as a conventional usage. Further, it can enhance the options of the metal wiring material in the TFT-LCD. Besides, the delay phenomena of the resistor capacitor RC can be decreased.

For a more complete understanding of the present invention

and for further advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawing, in which:

Brief Description of the Drawings

Graphs A-Z of Figure 1 is one of the preferred embodiments according to the present invention showing the structure of each process in the manufacturing steps; and

Figure 2 is the circuit diagram using the present invention to make.

Detailed Description of the Preferred Embodiments

Please referring to Figure 1A, it is one of the preferred embodiments according to the present invention showing step one. First, it uses the mask to define the position of the gate electrode metal wiring on the substrate 100. Then, it forms an A-Si seed layer 115 on the position. More, the ion of desired-plated metal and the graphs of the desired-plated area which being made by stronger oxidation—reduction materials processes ion replacement, and forms the gate electrode 11. The ion of the desired metal can be Cu, Al, Ag, Ni, Ti, W, and Mo. The desired-plated graph of made from the stronger reduction materials can be A-Si seed layer 115. Then, it processes the deposition on the dielectric layer 205, A-Si layer 215, and N^+ Si

layer 225. Please referring to Figure 1B, it is one of the preferred embodiments showing step two. The A-Si layer can use as a conducting channel, the N^+ Si layer can use as an ohm contact layer. The above deposition process forming the dielectric layer 205, A-Si layer 215, N^+ Si layer 225 can use some deposition methods, which include, physical vapor deposition PVD, low pressure chemical vapor deposition LPCVD, OR plasma enhanced chemical vapor deposition PECVD, and etc..

Following the above step, it completes the deposition of the N^+ Si layer. Please referring to Figure 1C, it is one of the preferred embodiments according to present invention showing step three. It defines the contact window 12, and shields the partial N^+ Si layer 225 against entering the masking process by using multiple photo-resists 305. Then, it processes lithography etching for removing un-photo- resist-shielding place thereto forming multiple contact windows 12. Then, please referring to Figure 1D, it is one of the preferred embodiments according to the present invention showing step 4 of the manufacturing process. After that, the photo-resist lift-off is processed for implementing the contact window. Please referring to Figure 1E, it is one preferred embodiment of the present invention showing step five, and the transparent conducting layer 405. The transparent conducting layer 405 can process deposition by the above deposition method. Besides, the material of the transparent conducting layer can be

ITO or IZO. Then, it defines the second metal wiring layer on the transparent conducting layer.

Accordingly, please referring Figure 1F, it is one of the preferred embodiments according to present invention showing step six. First, it forms the photo-resist 505, and defines the position of the second metal wiring. In the mean time, the source electrode and the drain electrode are defined. Then, it processes the masking process, lithography etching technique. The partial transparent conducting layer is removed thereto exposures partial N^+ Si layer as a N^+ seed layer 407. The N^+ Si seed layer 497 has the reaction ability with the material of the wiring metal to implement the replacement. The replacement reaction of the wiring metal and the N^+ Si seed layer 407 can be the replacement reaction of same type metals or the addition reaction. Please referring to Figure 1G, it is one of the preferred embodiments according to present invention showing step seven. It processes reaction by the chemical electric potential difference of the two substances thereto the second metal wiring 408 is formed on the exposure place of the N^+ Si seed layer 407. The place covered with residue transparent conducting layer cannot have second metal wiring 408 on it, but has a self-alignment. More, the chemical reaction can use electrical plating or non-electrical plating method to implement. Then, please referring to Figure 1H, it is one of the preferred embodiments according to present

invention showing step eight as well as presenting the second metal wiring 408 layout implement.

Next step, please referring to Figure I, it is one of the preferred embodiments according to present invention showing step nine as well as defining the wiring channel. It uses photo-resist 605 to shield the position of non-wiring channel. The photo-resist can be a positive-type photo-resist. After entering the masking process, the lithography etching is processed for forming wiring channel 227. Please referring to Figure 1 J, it is one of the preferred embodiments according to present invention showing ten. The wiring channel is implemented and the passivation layer is formed finally. Please referring to Figure 1K, it is one of the preferred embodiments according to present invention showing step eleven. By using the above deposition method, it deposits a passivation layer, and then the fourth photo-resist 710 is placed on the component. More, the passivation layer 700 without the fourth photo-resist covering is removed for forming the component passivation layer 706. Further, the fourth photo-resist 710 is removed. Please referring to Figure 1L, it is one of the preferred embodiments according to present invention showing twelve as well as showing the manufacture of the TFT array.

Please referring to Figure 2, it is the circuit diagram using the present invention to make. From description of the circuit diagram, the first masking process is processed firstly for forming the first

metal wiring 11. Also, it defines the position of the gate electrode. The wiring metal of the gate electrode is used the replacement method to implement. Then, it uses the definition of the second masking process to form a signal area and the contact window thereto deposit the transparent conducting layer 14. Further, the third masking process is processed to define the source electrode and the drain electrode 13. The wiring metal can be partial N^+ Si layer in order to process the self-alignment replacement reaction for the seed. More, the fourth masking process is processed for forming a wiring channel 17. Then, the fifth masking process is processed for forming a passivation layer 15. The method of fabricating thin film transistor TFT according to the present invention more focuses on the gate in initial forming status and the third masking process. It uses the oxidation-reduction character of the chemical plating method to form a metal wiring for implementing the metal wiring layout of the TFT-LCDs. Further, it can avoid the exposure of the metal wiring happening in the masking process as well as the component defect occurring.

In conclusion, the present invention meets novelty, improvement, and is applicable to the industry. It therefore meets the essential elements in patentability. There is no doubt that the present invention is legal to apply to the patent, and indeed we hope that this application can be granted as a patent.

Although the present invention has been described in detail

with respect to alternate embodiments, various changes and modifications may be suggested to one skilled in the art, and it should be understood that various changes, suggestions, and alternations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.